Amendments to the Claims:

Please amend claims 1 and 9. The claims are as follows:

Listing of Claims:

1. (Currently Amended) A cyclic redundancy check circuit, comprising:

a W-bit packet data slice latch having outputs;

a multiple level XOR subtree having inputs and outputs, each level comprising one or more XOR subtrees, each output of said packet data slice latch coupled to an input of said multiple level XOR subtree, each lower level XOR subtree of said multiple level XOR subtree coupled to a higher level XOR subtree of said multiple level XOR subtree through an intervening latch level;

a remainder XOR subtree having inputs and outputs;

a combinational XOR subtree having inputs and outputs, the outputs of said remainder XOR subtree and the outputs of said multiple level XOR subtree coupled to the inputs of said combinational XOR subtree; and

an M-bit current CRC result latch having inputs and outputs, the output of said combinational XOR subtree coupled to the inputs of said current CRC result latch and the outputs of said M-bit current CRC result latch coupled to the inputs of said remainder XOR subtree.

2. (Original) The circuit of claim 1, wherein said packet data slice latch, all latches in said intervening latch levels and said current CRC remainder latch are responsive to the same clock signal.

3. (Original) The circuit of claim 1, wherein K, the maximum number of XOR stages comprised of Z-input XOR gates in said remainder XOR subtree is the smallest whole positive number greater than the log to the base Z of the largest number of bits I of a subset of the M-bits of said CRC result latch required to generate output bits of said remainder XOR subtree.

4. (Original) The circuit of claim 3, wherein the maximum number N of inputs to any XOR subtree in any level of said multiple level XOR subtree comprised of Z-input XOR gates is equal to K raised to the Z power.

5. (Original) The circuit of claim 4, wherein the number of levels of said multiple level XOR subtree (Y-1), is the smallest whole positive number greater than the log to the base N of the largest number of bits J of a subset of the W-bits of said packet data slice latch.

6. (Original) The circuit of claim 5, wherein W=2048, I=20, J=1059, Z=3, K=3 and N= 27.

7. (Original) The circuit of claim 1, wherein

the number of the number of levels of said multiple level XOR subtree is a function of A, the maximum number of input bits to said multiple level XOR subtree to give a single output bit of said multiple level XOR subtree and of B, the maximum number of input bits to said remainder XOR subtree to give a single output bit of said remainder XOR subtree.

8. (Original) The circuit of claim 7, wherein the number of the number of levels of said multiple level XOR subtree is the log to the base B of A.

9. (Original) (Currently Amended) A method for cyclic redundancy check calculation, comprising:

providing a W-bit packet data slice latch having outputs;

providing a multiple level XOR subtree having inputs and outputs, each level comprising one or more XOR subtrees, each output of said packet data slice latch coupled to an input of said multiple level XOR subtree, each lower level XOR subtree of said multiple level XOR subtree coupled to a higher level XOR subtree of said multiple level XOR subtree through an intervening latch level;

providing a remainder XOR subtree having inputs and outputs;

providing a combinational XOR subtree having inputs and outputs, the outputs of said remainder XOR subtree and the outputs of said multiple level XOR subtree coupled to the inputs of said combinational XOR subtree; and

providing an M-bit current CRC result latch having inputs and outputs, the output of said combinational XOR subtree coupled to the inputs of said current CRC result latch and the outputs of said M-bit current CRC result latch coupled to the inputs of said remainder XOR subtree.

10. (Original) The method of claim 9, wherein said packet data slice latch, all latches in said intervening latch levels and said current CRC remainder latch are responsive to the same clock signal.

11. (Original) The method of claim 9, wherein K, the maximum number of XOR stages comprised of Z-input XOR gates in said remainder XOR subtree is the smallest whole positive number greater than the log to the base Z of the largest number of bits I of a subset of the M-bits of said CRC result latch required to generate output bits of said remainder XOR subtree.

12. (Original) The method of claim 11, wherein the maximum number of inputs N to any XOR subtree in any level of said multiple level XOR subtree comprised of Z-input XOR gates is equal to K raised to the Z power.

13. (Original) The method of claim 12, wherein the number of levels of said multiple level XOR subtree (Y-1), is the smallest whole positive number greater than the log to the base N of the largest number of bits J of a subset of the W-bits of said packet data slice latch.

14. (Original) The method of claim 13, wherein W=2048, I=20, J=1059, Z=3, K=3 and N= 27.

15. (Original) The method of claim 9, wherein the number of the number of levels of said multiple level XOR subtree is a function of A, the maximum number of input bits to said multiple level XOR subtree to give a single output bit of said multiple level XOR subtree and of B, the maximum number of input bits to said remainder XOR subtree to give a single output bit of said remainder XOR subtree.

16. (Original) The method of claim 15, wherein the number of the number of levels of said multiple level XOR subtree is the log to the base B of A.

17. (Original) A method of designing an M-bit cyclic redundancy check circuit, the method comprising:

partitioning an XOR function of said cyclic redundancy check circuit into a remainder XOR partition and a multiple level packet data slice XOR partition;

determining I, the largest number of bits I of a subset of the M-bits of a CRC result required to generate output bits of a remainder partition XOR subtree of said cyclic redundancy check circuit;

determining Z, the largest number of inputs to an XOR gate in a design library to be used in said cyclic redundancy check circuit;

calculating K, the maximum number of XOR stages comprised of Z-input XOR gates in said remainder XOR subtree;

calculating N, the maximum number of inputs to any XOR subtree in any level of a multiple level XOR subtree partition of said cyclic redundancy check circuit;

partitioning said multiple level XOR subtree partition into XOR subtrees having no number of inputs that is larger than a number of inputs to said remainder XOR subtree; and

inserting a latch between each XOR subtree of a lower level partition of said packet data slice XOR partition and an immediately higher level partition of said packet data slice XOR partition.

18. (Original) The method of claim 17, wherein K is the smallest whole positive number greater than the log to the base Z of I.

19. (Original) The method of claim 18, wherein N, is equal to K raised to the Z power.

20. (Original) The method of claim 19, wherein the number of levels of said packet data slice XOR partition (Y-1), is the smallest whole positive number greater than the log to the base N of the largest number of bits J of a subset of the W-bits of said packet data slice latch.

Amendments to the Drawings:

The attached sheet of drawings includes changes to FIG. 3. This sheet, which includes FIG. 3 replaces the original sheet including FIG. 3. In FIG. 3, the label of elements 310 have been changed to from "N BY N-WAY LEAF XOR SUBTREE" to "M BY N-WAY LEAF XOR SUBTREE" to correct a typographical error in the label. This change matches the text on line page 9, s 10-11 of the specification.

Attachment: Replacement Sheet

CONCLUSION

If Examiner believes that anything further would be helpful, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below.

Respectfully submitted,

Dated: 04/27/2004

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